Poster Contributions

[P1] Tatsuro Sugiura, Yuki Yamanashi, and Nobuyuki Yoshikawa (Yokohama National University)
Demonstration of 30 GHz generation of truly random numbers using superconductive circuit

[P2] Takeyuki Tanaka, Jun Saito, Tadayuki Kobayashi, Masataka Moriya, Yoshinao Mizugaki (University of Electro-Communications), and Masaaki Maezawa (AIST)
Design and Operation of the Voltage Multiplier Cell with a Stacked-SQUID

[P3] Yuki Yamanashi, Ichiro Okawa, and Nobuyuki Yoshikawa (Yokohama National University)
Design Approach of Dynamically Reconfigurable Single Flux Quantum Logic Circuits

[P4] D. Ozawa, Y. Natsume, Y. Yamanashi, and N. Yoshikawa (Yokohama National University)
Design and Evaluation of Multi-Flux Drivers Using High Bc Junctions

[P5] Irina Kataeva, Hiroyuki Akaie, and Akira Fujimaki (Nagoya University)
Clocking considerations for an SFQ Reconfigurable Data Paths processor

[P6] Tao Xue, Park Heejoung, Yuki Yamanashi, and Nobuyuki Yoshikawa (Yokohama National University)
Stabilization of Josephson Latching Driver using Series Inductances

[P7] Masamitsu Tanaka, Kazuyoshi Takagi, and Naofumi Takagi (Nagoya University)
Miniaturization of SFQ Floating-point Processing Units Using Variable-length Shift-registers

[P8] Kazumasa Umeda, Yuki Yamanashi, and Kiyoto Sai (Yokohama National University)
Superconductive Combinational Logic Circuit Using Magnetically Coupled SQUID Array

[P9] Kiyoshi Minami, Yuki Yamanashi, and Nobuyuki Yoshikawa (Yokohama National University)
Design of a single-flux quantum majority logic gate

[P10] Shimojima, Yuki Yamanashi, and Nobuyuki Yoshikawa (Yokohama National University)
Consideration of a digital SQUID with positive magnetic feedback

[P11] Y. Natsume, D. Ozawa, Y. Yamanashi, and N. Yoshikawa (Yokohama National University)
Chip-to-Chip Communication using Inductive Coupling

[P12] H. Suzuki, Y. Yamanashi, and N. Yoshikawa (Yokohama National University)
Design of 2 × 2 switch using PTL-connectable logic cells

[P13] Y. Okamoto, H. Park, H. Jin, K. Yaguchi, Y. Yamanashi, N. Yoshikawa (Yokohama National University), and T. Van Duzer (UC Berkeley)
Access Time Measurement of 64 kb Josephson/CMOS Hybrid Memories by using SFQ Time-to-Digital Converter

[P14] Y. Takahashi, H. Suzuki, Y. Yamanashi, and N. Yoshikawa (Yokohama National University)
Design of Input Circuits for SFQ Multi-Stop Time-to-Digital Converters for Time-of-Flight Mass Spectrometry

Fabrication of NbN Josephson Junctions with Plasma-Nitried AlN Barriers Formed by RF Substrate Biasing

[P16] Ryo Kasagi, Masamitsu Tanaka, Kataeva Irina, Masato Ito, Hiroyuki Akaie, and Akira Fujimaki (Nagoya University)
Evaluation of an SFQ-ALU circuit based on the Advanced Process 2

[P17] Masato Ito, Masamitsu Tanaka, Kataeva Irina, Ryo Kasagi, Masakazu Okada, Tomohito Koketsu, Hiroyuki Akaike, and Akira Fujimaki (Nagoya University)
A 4x4 SFQ switch circuit based on a Nb multi-layer process

[P18] Shigeyuki Miyajima (Nagoya University), Thomas Ortlepp (Ilmenau University of Technology), Ali Bozbey (TOBB Economy and Technology University), and Akira Fujimaki (Nagoya University)
Experimental analysis of gray zones in quasi-one-junction SQUIDs

[P19] Motoki Sato, Masamitsu Tanaka, Kazuyoshi Takagi, and Naofumi Takagi (Nagoya University)
A Verification Method for Pipeline Processing Behavior of Single-Flux-Quantum Circuits by Equivalence Checking of Timed Logic Formulae

[P20] S. Miura, N. Takeuchi, Y. Yamanashi, and N. Yoshikawa (Yokohama National University)
Improvement in SFQ Circuit Measuring Escape Rate in Josephson Junction

Design of RSFQ Circuits for Controlling Superconducting Qubits

[P22] Yoshiki Arita, Yuki Yamanashi, Toshihiko Baba, Nobuyuki Yoshikawa (Yokohama National University)
Integration of optical waveguides with SFQ circuits

[P23] Toshiki Kainuma, Fumishige Miyaoka, Yasuhiro Shimamura, Yuki Yamanashi, and Nobuyuki Yoshikawa (Yokohama National University)
Proposal of Resettable Muller-C gates Using Single-Flux-Quantum Circuits

[P24] K. Yaguchi, Y. Okamoto, H. Jin, H. Park, Y. Yamanashi, N. Yoshikaw (Yokohama National University), and T. Van Duzer (UC Berkeley)
Implementation of a Self-Bias Circuit for Josephson-CMOS Hybrid Memories

Booth encoder for large scale integration SFQ circuits

[P26] K. Shigehara, H. Akaike, and A. Fujimaki (Nagoya University)
Variation of Inductance Using Magnetic Nanoparticles toward SFQ Device Applications

Investigation of High-Speed CMOS Differential Amplifier for Josephson/CMOS Hybrid Memory Systems

Design of SFQ Half-Precision Floating-Point Multipliers Using 10 kA/cm2 Nb Multi-Layer Process

[P29] Y. Niihara, Y. Iwata, and M. Naito (Tokyo University of Agriculture and Technology)
Growth of MgB2 ultra thin films

[P30] H. Sawaki, and M. Naito (Tokyo University of Agriculture and Technology)
MgB2 thin film growth by modified hybrid physical chemical deposition with a pocket heater