**6th Superconducting SFQ VLSI Workshop (SSV 2013)**

**Technical Program**

*Venue: National Institute of Advanced Science and Technology (AIST), Tsukuba, Japan*

**Thursday, November 21st**

13:00-13:05 **Opening Remarks**  
M. Hidaka

13:05-14:25 **Session I**

13:05-13:45 **[INV-1]**  
S. Holmes (Invited), *Booz Allen Hamilton.*  
“Large-Scale Superconducting Computing in the USA: Prospects and Status”

13:45-14:25 **[INV-2]**  
H. Rogalla (invited), *Univ. of Colorado/Univ. of Twente.*  
“Thoughts about the Future of Superconducting Electronics”

14:25-14:45 **Coffee Break**

14:45-15:55 **Session II**

14:45-15:10 **[INV-3]**  
C. Fourie (Invited), *Stellenbosch Univ.*  
“Layout Verification of Superconductive Integrated Circuits”

15:10-15:25 **[O-1]**  
Nobutaka Kito, *Chukyo Univ.*  
“Retiming of SFQ Logic Circuits for Reduction of Flip-flops”

15:25-15:40 **[O-2]**  
M. Tanaka, *Nagoya Univ.*  
“Design and Implementation of Component Circuits for RSFQ Bit-slice Microprocessors”

15:40-15:55 **[O-3]**  
Y. Yamanashi, *Yokohama National Univ.*  
“Circuit Design of Zero-Static Power SFQ Circuit Using Magnetic Flux Biasing”

16:00-17:30 **Poster Session**

**[P-1]**  
Y. Urai, *Univ. of Electro-Communications*  
“Mutually-Coupled Dc/SFQ Converter Tested Using an On-Chip Pulse Generator”

**[P-2]**  
Y. Tsuji, *Tohoku Univ.*  
“Characteristics of rf-SQUID Ladder Circuits”

**[P-3]**  
K. Sato, *Yokohama National Univ.*  
“Design and Implementation of a High Sensitive DC/SFQ Converter”

**[P-4]**  
X. Peng, *Yokohama National Univ.*  
“Improvement of Interface for Josephson/CMOS Hybrid Memory on Anti-Ground-Current and Low Power Dissipation”
“New Design Method of Single Flux Quantum Logic Circuits Using Dynamically Reconfigurable Logic Gates”

“Comparative Study of SFQ Parallel Multipliers”

“Improvement of Performance of a Superconductive Random Number Generator by Optimization of Parameters”

“Improvement of Slew Rate of High-Sensitive Superconductive Digital Magnetometer”


“Design and Test of Basic Cells for Adiabatic Quantum-Flux-Parametron Logic with Magnetic-Shielding Structures”

“Design of an SFQ Butterfly Circuit with Signed Number Operation Using the 10 kA/cm2 Process”

“Improvement of Decoder and Data Drivers in Terms of Power Consumption for 64-kb SFQ/CMOS Hybrid memories”


“Asymmetric-Nanobridge-SQUIDs Based on High-Temperature Superconductors”

“Evaluation of Serially Biased SFQ Circuits Using Floating Ground Plane Structures”

“Logical Design of Bit-Slice Barrel Shifter for 32-bit SFQ Microprocessor”

“A Design Framework for SFQ Circuits using Clockless Gates”

“Development of Low-power Shift-register Memories with Josephson Junction Biasing for SFQ Micro Processor”
“High-Speed Demonstration of an SFQ Bit-Serial Floating-Point Adder Using 10 kA/cm2 Nb Process”


[P-21] T. Takinami, Nagoya Univ.

“Experimental Evaluation of Effect of Noise Reduction Technique in Low Critical Current RSFQ Circuits”

[P-23] Y. Guowei, Nagoya Univ.
“High-Frequency Response Characteristics of the Neutron Detector with the One-Way Traffic Structure”

“Design of Josephson RAM based on Nb 10kA/cm^2 Advanced Process”

[P-25] H. Nakagawa, Saitama Univ.
“Design of SFQ Logic Cells with Magnetic Shield Structure for Digital SQUID”

[P-26] D. Si, Yokohama National Univ.
“Yield Analysis of Large-scale Adiabatic Quantum Flux Parametoron Logic: the Effect of the Deviation of the Inductance Parameter”

18:00-19:30 Banquet at LEOC Restaurant (AIST Tsukuba Center No.1 bldg. 2F)

Friday, November 22nd
9:00-10:35 Session III
9:00-9:25 [INV-4] M. Ohkubo (Invited), AIST
“Breakthrough in Analytical Sciences by Superconducting Analog and Digital Devices”

“Research Results of CREST-JST SFQ-RDP Project and Future Issues”

“Several Applications using Quantum-Flux-Latch”

“Investigation of Small Size Trilayer Josephson Junctions”
“The Influence of Pd1-xNix Alloys on the Magnetic Field Characteristics of SQUIDs”

10:35-10:55 Coffee Break

10:55-11:55 Session IV-
“SFQ Readout Circuit for Photon-number Resolving SNSPDs”
“Evaluation of Operating Frequency in Small SNSPDs with SFQ Readout Circuits”
“Development of Single-Chip Voltage Waveform Generators Based on SFQ Pulse-Frequency Modulation”
“Design of an Integrated Quantum Voltage Noise Source for Johnson Noise Thermometry”

11:55-12:00 Announcement of SSV 2014 for Young Scientist M. Tanaka

12:00-12:05 Closing Remarks A. Fujimaki