9th Superconducting SFQ VLSI Workshop (SSV 2016)

Technical Program

Venue: Media Hall in Central Library, Yokohama National University, Yokohama, Japan

Tuesday, August 2

13:00 – 13:10  Opening Remarks  N. Yoshikawa

13:10 – 15:35  Oral Session I  Media Hall

13:10 – 13:50[I-1] (Invited) A. Kirichenko (HYPRES)  
"LSI Design of Energy Efficient ERSFQ Circuits"

13:50 – 14:30[I-2] (Invited) C. Fourie (Stellenbosch University)  
"Lumped-Element Extraction of Impedance Discontinuities in Superconducting Circuit Interconnect Lines"

14:30 – 14:50  Coffee Break

14:50 – 15:05[O-1] C. L. Ayala, N. Takeuchi (Yokohama National University), T. Ortlepp (CiS Research Institute), Y. Yamanashi and N. Yoshikawa (Yokohama National University)  
"Kogge-Stone and Brent-Kung Adders Optimized for Adiabatic Quantum-Flux-Parametron Majority Logic"

"Eight-Bit Bit-Serial RSFQ Microprocessor with Minimal Instruction Set Architecture for Demonstration Programs"

“A Microarchitecture of an RSFQ 4-Bit Bit-Slice 32-Bit Processor”
15:35 – 16:55 Short Poster Presentation  
*Media Hall*

17:30 – 18:30 Banquet  
*Cafeteria 2*

**Wednesday, August 3**

10:00 – 11:30 Poster Session  
*Information Lounge*

[P-1] M. Tanaka, H. Akaike and A. Fujimaki (Nagoya University)  
“Computer-Aided Design for RSFQ Standard Cell Layouts”

[P-2] T. Ono, H. Suzuki, Y. Yamanashi and N. Yoshikawa (Yokohama National University)  
“Design and Demonstration of Component Circuits for an SFQ-Based Single-Chip FFT Processor”

[P-3] Y. Murai, C. Ayala, N. Takeuchi, Y. Yamanashi and N. Yoshikawa (Yokohama National University)  
“Towards VLSI Design and Development of AQFP EDA Software Considering 1 mm Wire Limitation”

[P-4] N. Kito, G. Matsumoto (Chukyo University), K. Takagi and N. Takagi (Kyoto University)  
“Extension of a Logic Simulation System for Simulation-Based Verification of RSFQ Logic Circuits”

[P-5] R. Sato, T. Ono, Y. Yamanashi and N. Yoshikawa (Yokohama National University)  
“50 GHz Demonstration of a Complex Event Detector Unit for Complex Event Processing Systems Using the Nb 10 kA/cm² Josephson Process”

[P-6] K. Sano, Y. Abe, Y. Yamanashi and N. Yoshikawa (Yokohama National University)  
“Reduction of Supply Current and Capacity Enlargement of First-In First-Out Buffers in Single-Flux-Quantum Time-to-Digital Converters”

[P-7] T. Wakamatsu, Y. Yamanashi and N. Yoshikawa (Yokohama National University)  
“Analysis of Influences of Thermal Noises on Performance of Superconductive Σ-Δ A/D Converter”

[P-9] K. Fang, N. Takeuchi, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Proposal of Multi-Logic-Stage AQFP Circuits”

[P-10] S. Kobako, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Design of Adiabatic-Quantum-Flux-Parametron Autocorrelator for Submillimeter-Wave Spectrometry”

[P-11] Q. Xu, C. L. Ayala, N. Takeuchi, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“HDL-Based Cell Library for AQFP Logic Using 4-Phase Clock”

[P-12] T. Igarashi, H. Suzuki, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Design and Evaluation of Unipolar VTM Cell and Superconductor Loop Drivers”

[P-13] Y. Abe, K. Sano, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Experimental Evaluation of Josephson Comparators for Small Current Detection”

“Design of a Look-Up Table Based on the Dual-Rail Single Flux Quantum Circuit with Ferromagnetic Materials”

[P-15] H. Takayama, N. Tsuji, N. Takeuchi, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Proposal of a Random Access Memory Cell Composed of Quantum Flux Parametron”

[P-16] G. Konno, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Demonstration of 64-kb Josephson-CMOS Hybrid Memories with SFQ Inputs and Outputs”

[P-17] F. China, N. Tsuji, N. Takeuchi (Yokohama National University), T. Ortlepp (CiS Research Institute), Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Demonstration of Data Transmission on Long Interconnections between Adiabatic Quantum-Flux-Parametron Gates Using Passive Transmission Lines”
“Characteristics of Low-Voltage Vortex Transitional Memory Developed with Nb 4-Layer, 10-kA/cm² Fabrication Process”

[P-19] N. Tsuji, C. Ayala, N. Takeuchi (Yokohama National University), T. Ortlepp (CiS Research Institute), Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Design and Implementation of an 8-Word by 1-Bit Register File Using Adiabatic Quantum Flux Parametron Logic”

[P-20] H. Imai, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Simulation and Measurement of Influence of Flux Quantum Trapped in Moat on Superconducting Integrated Circuit”

[P-21] K. Ota, M. Naruse, T. Taino, H. Myoren (Saitama University), L. Kang, J. Chen and P. Wu (Nanjing University)
“SFQ Read-out Circuit Using Inductive Coupling for Photon-Number-Resolving SNSPD Array”

[P-22] T. Matsushima, T. Ortlepp (CiS Research Institute), N. Takeuchi, Y. Yamanashi, N. Yoshikawa (Yokohama National University)
“Investigation of Gray Zone Width of Adiabatic Quantum Flux Parametron”

[P-23] S. Muramatsu, Y. Yamanashi and N. Yoshikawa (Yokohama National University)
“Study on Superconductive Associative Memory”

11:30 – 13:00  Lunch

13:00 – 14:25  Oral Session II  Media Hall

13:00 – 13:40[I-3] (Invited) S. Razmkhah and A. Bozbey (TOBB University of Economics and Technology)
“Demonstration of a Different Single Flux Quantum Logic and Arithmetic Sub-Circuits for Custom Designed Parallel Pipe-line Microprocessor in Cryocooler Environment”

“Noise Performance of Digital SQUID Magnetometer Using DROS Comparator”
“Thermally-Fluctuated SFQ Pulse Intervals Observed in IO Characteristics of a Double-Flux-Quantum Amplifier”

“Towards Robust Coupled Field Induced Josephson Junctions”

14:25 – 14:45 Coffee Break

14:45 – 16:25 Oral Session III Media Hall

14:45 – 15:25 [I-4] (Invited) N. Takeuchi, C. L. Ayala, Q. Xu, F. China, N. Tsuji, T. Ando, Y. Murai, K. Fang, Y. Yamanashi, N. Yoshikawa (Yokohama National University) and T. Ortlepp (CiS Research Institute)
“A Review of Current Progress of Adiabatic Quantum-Flux-Parametron Logic”

“First Demonstration of Double-Active-Layered AQFP Circuits Using Double Gate Process”

“Yield Improvement of Nb 9-Layer Advanced Process Using PECVD SiO₂ Insulator”


16:25 – 16:35 Closing Remarks M. Hidaka